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奇美電子 CHIMEI INNOLUX

PRODUCT SPECIFICATION

□ Tentative Specification
□ Preliminary Specification
■ Approval Specification

MODEL NO.: V315H3
SUFFIX: L02

Customer:

APPROVED BY **SIGNATURE**

Name / Title _____ _____

Note

Please return 1 copy for your confirmation with your signature and comments.

Approved By	Checked By	Prepared By
Chao-Chun Chung	Josh Chi	**Edouard Huang**

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REVISION HISTORY

Version	Date	Page(New)	Section	Description
Ver. 2.0	Apr. 13, 2011	All	All	The Approval specification was first issued.

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1. GENERAL DESCRIPTION

1.1 OVERVIEW

V315H3-L02 is a 31.5" TFT Liquid Crystal Display module with 4U-type CCFL Backlight unit and **2ch**-LVDS interface. This module supports 1920 x 1080 Full HDTV format and can display 16.7M colors (8-bit). The inverter module for backlight is built-in.

1.2 FEATURES

-High brightness (450 nits)
- Ultra-high contrast ratio (6000:1)
- Fast response time (gray to gray average 8.5ms)
- High color saturation NTSC 72%
- Full HDTV (1920 x 1080 pixels) resolution, true HDTV format
- Ultra wide viewing angle : 176(H)/176(V)(CR≥20)with Super MVA technology
- DE (Data Enable) only mode
- LVDS (Low Voltage Differential Signaling) interface
- Optimized response time for 60Hz frame rate
- Color reproduction (nature color)
- Low color shift function
- RoHs compliance

1.3 APPLICATION

- TFT LCD TVs
- Multi-Media Display

1.4 GENERAL SPECIFICATIONS

Item	Specification	Unit	Note
Active Area	698.4 (H) x 392.85 (V) (31.51" diagonal)	mm	(1)
Opening Area	703.8 (H) x 399.0 (V)	mm	
Driver Element	a-si TFT active matrix	-	
Pixel Number	1920 x R.G.B. x 1080	pixel	
Pixel Pitch(Sub Pixel)	0.12125 (H) x 0.36375 (V)	mm	
Pixel Arrangement	RGB vertical stripe	-	
Power consumption	74	W	
Display Colors	Transmissive mode / Normally black	-	
Display Operation Mode	Anti-Glare coating (Haze 11%),Hard coating (3H)	-	
Surface Treatment	Anti-Glare coating (Haze 11%),Hard coating (3H)	mm	(1)

Note (1) Please refer to the attached drawings in chapter 9 for more information about the front and back outlines.

Note (2) Please refer sec 3.1 and 3.2 for more information of Power consumption

Note (3) The spec. of the surface treatment is temporarily for this phase. CMI reserves the rights to change this feature.

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1.5 MECHANICAL SPECIFICATIONS

Item		Min.	Typ.	Max.	Unit	Note
Module Size	Horizontal (H)	759	760	761	mm	(1)
	Vertical (V)	449	450	451	mm	(1)
	Depth (D)	41	42	43	mm	(2)
	Depth (D)	53.8	54.8	55.8	mm	(3)
Weight			5211		g	-

Note (1) Please refer to the attached drawings for more information of front and back outline dimensions.

Note (2) Module Depth is between bezel to T-CON cover.

Note (3) Module Depth is between bezel to Inverter cover.

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2. ABSOLUTE MAXIMUM RATINGS

2.1 ABSOLUTE RATINGS OF ENVIRONMENT

Item	Symbol	Value		Unit	Note
		Min.	Max.		
Storage Temperature	TST	-20	+60	ºC	(1)
Operating Ambient Temperature	TOP	0	50	ºC	(1), (2)
Shock (Non-Operating)	SNOP	-	50	G	(3), (5)
Vibration (Non-Operating)	VNOP	-	1.0	G	(4), (5)

Note (1) Temperature and relative humidity range is shown in the figure below.

(a) 90 %RH Max. (Ta ≦ 40 ºC).

(b) Wet-bulb temperature should be 39 ºC Max. (Ta > 40 ºC).

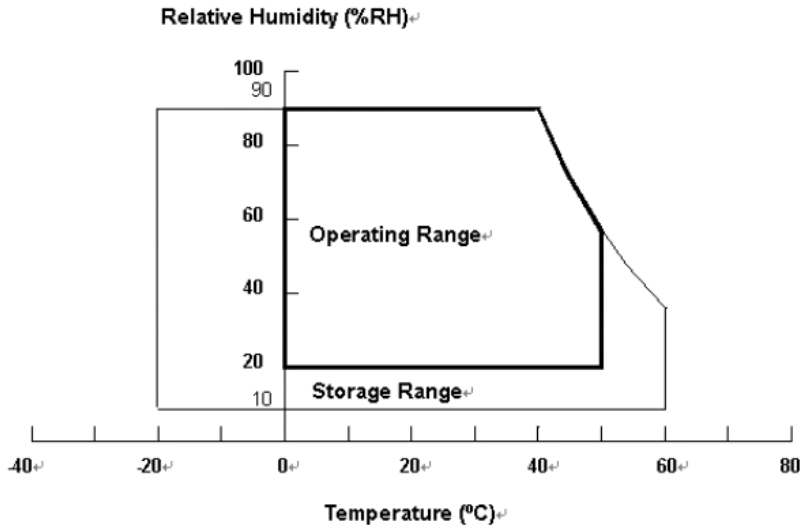
(c) No condensation.

Note (2) The maximum operating temperature is based on the test condition that the surface temperature of display area is less than or equal to 65 ºC with LCD module alone in a temperature controlled chamber. Thermal management should be considered in final product design to prevent the surface temperature of display area from being over 65 ºC. The range of operating temperature may degrade in case of improper thermal management in final product design.

Note (3) 11 ms, half sine wave, 1 time for ± X, ± Y, ± Z.

Note (4) 10 ~ 200 Hz, 10 min, 1 time each X, Y, Z.

Note (5) At testing Vibration and Shock, the fixture in holding the module has to be hard and rigid enough so that the module would not be twisted or bent by the fixture.



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2.2 PACKAGE STORAGE

When storing modules as spares for a long time, the following precaution is necessary.

(a) Do not leave the module in high temperature, and high humidity for a long time, It is highly recommended to store the module with temperature from 0 to 35 ℃ at normal humidity without condensation.

(b) The module shall be stored in dark place. Do not store the TFT-LCD module in direct sunlight or fluorescent light.

2.3 ELECTRICAL ABSOLUTE RATINGS

2.3.1 TFT LCD MODULE

Item	Symbol	Value		Unit	Note
		Min.	Max.		
Power Supply Voltage	VCC	-0.3	13.5	V	(1)
Logic Input Voltage	VIN	-0.3	3.6	V	

2.3.2 BACKLIGHT INVERTER UNIT

Item	Symbol	Value		Unit	Note
		Min.	Max.		
Lamp Voltage	V	—	3000	VRMS	
Power Supply Voltage	VBL	0	30	V	(1)
Control Signal Level	—	-0.3	7	V	(1), (3)

Note (1) Permanent damage to the device may occur if maximum values are exceeded. Function operation should be restricted to the conditions described under Normal Operating Conditions.

Note (2) No moisture condensation or freezing.

Note (3) The control signals include On/Off Control, External PWM Control and DET_5V signal for inverter status output.

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3. ELECTRICAL CHARACTERISTICS

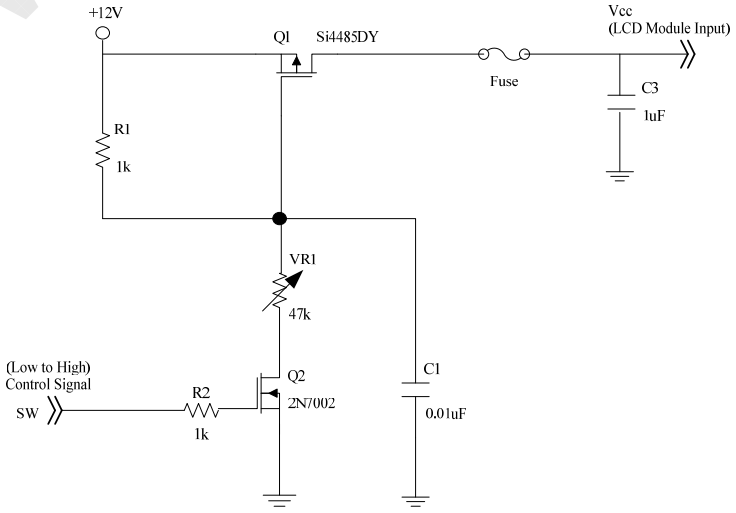
3.1 TFT LCD MODULE

(Ta = 25 ± 2 ºC)

Parameter			Symbol	Value			Unit	Note
				Min.	Typ.	Max.		
Power Supply Voltage			V_{CC}	10.8	12	13.2	V	(1)
Rush Current			I_{RUSH}	–	–	3.5	A	(2)
Power consumption		White Pattern	P_T	–	4.18	5.16	W	(3)
		Black Pattern		–	4.03	4.8		
		Horizontal Stripe		–	6.48	8.16		
Power Supply Current		White Pattern	–	–	0.35	0.43	A	(3)
		Black Pattern	–	–	0.34	0.40	A	
		Horizontal Stripe	–	–	0.54	0.68	A	
LVDS interface	Differential Input High Threshold Voltage		V_{LVTH}	+100	–	–	mV	(4)
	Differential Input Low Threshold Voltage		V_{LVTL}	–	–	-100	mV	
	Common Input Voltage		V_{CM}	1.0	1.2	1.4	V	
	Differential input voltage (single-end)		$\|V_{ID}\|$	200	–	600	mV	
	Terminating Resistor		R_T	–	100	–	ohm	
CMIS interface	Input High Threshold Voltage		V_{IH}	2.7	–	3.3	V	
	Input Low Threshold Voltage		V_{IL}	0	–	0.7	V	

Note (1) The module should be always operated within the above ranges.

Note (2) Measurement Conditions:



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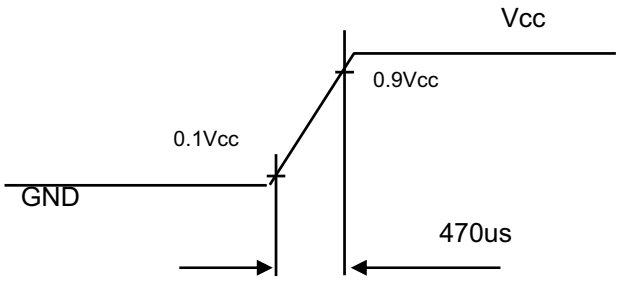
Vcc rising time is 470us



Note (3) The specified power supply current and power consumption is under the conditions at Vcc = 12 V, Ta = 25 ± 2 ºC, f_v = 60 Hz, whereas a power dissipation check pattern below is displayed.

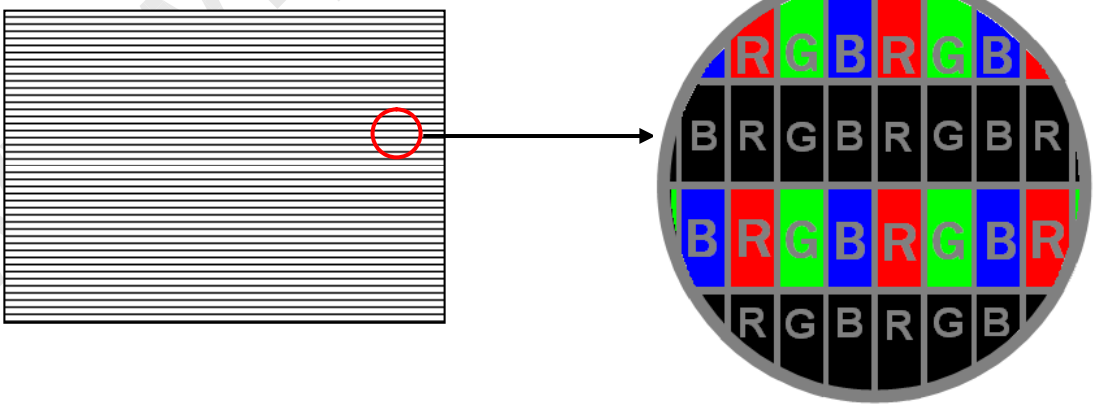
a. White Pattern

Active Area

b. Black Pattern

Active Area

c. Horizontal Pattern



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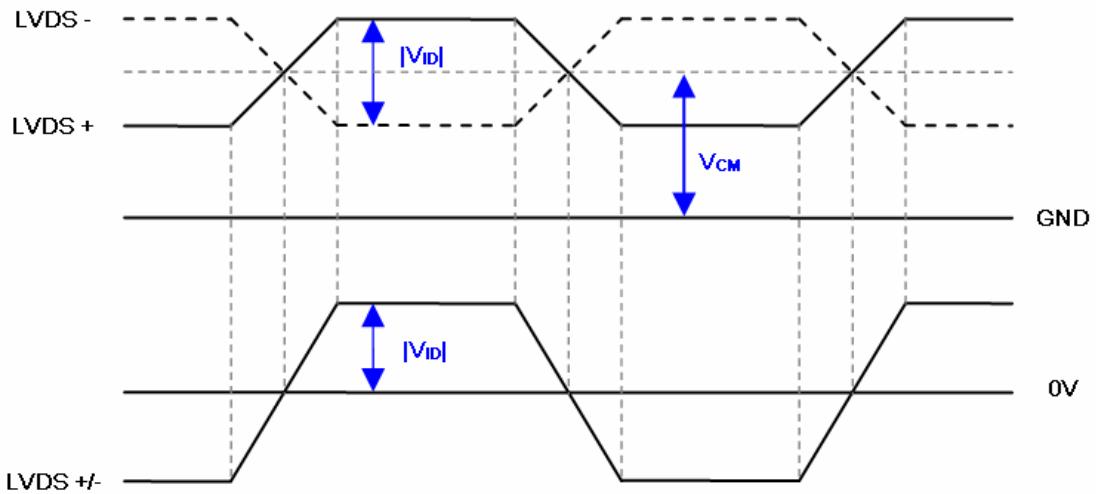
Note (4) The LVDS input characteristics are as follows :



3.2 BACKLIGHT CONNECTOR PIN CONFIGURATION

3.2.1 CCFL (Cold Cathode Fluorescent Lamp) CHARACTERISTICS (Ta = 25 ± 2 ºC)

Parameter	Symbol	Value			Unit	Note
		Min.	Typ.	Max.		
Lamp Input Voltage	V_L	-	1560	-	V_{RMS}	
Lamp Current	I_L	11.8	12.3	12.8	mA_{RMS}	(1)
Lamp Turn On Voltage	V_S	-	-	2710	V_{RMS}	Ta = 0 ºC (2)
		-	-	2260	V_{RMS}	Ta = 25 ºC (2)
Operating Frequency	F_L	40	-	70	KHz	(3)
Lamp Life Time	L_{BL}	50,000	60,000	-	Hrs	(4)

3.2.2 INVERTER CHARACTERISTICS (Ta = 25 ± 2 ºC)

Parameter	Symbol	Value			Unit	Note
		Min.	Typ.	Max.		
Total Power Consumption	P_{IP}	-	74	78	W	(5), (6), IL =12.3mA
Power Supply Voltage	V_{BL}	22.8	24	25.2	V_{DC}	
Power Supply Current	I_{BL}	-	3.08	3.25	A	Non Dimming
Input Ripple Noise	-	-	-	912	mV_{p-p}	V_{BL}=22.8V
Oscillating Frequency	F_W	60	63	66	KHz	(3)
Dimming Frequency	F_B	150	160	170	Hz	
Minimum Duty Ratio	D_{MIN}	10	20		Hz	(7)

Note (1) Lamp current is measured by utilizing AC current probe and its value is average by measuring master and slave board.:

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Note (2) The lamp starting voltage V_S should be applied to the lamp for more than 1 second after startup. Otherwise the lamp may not be turned on.

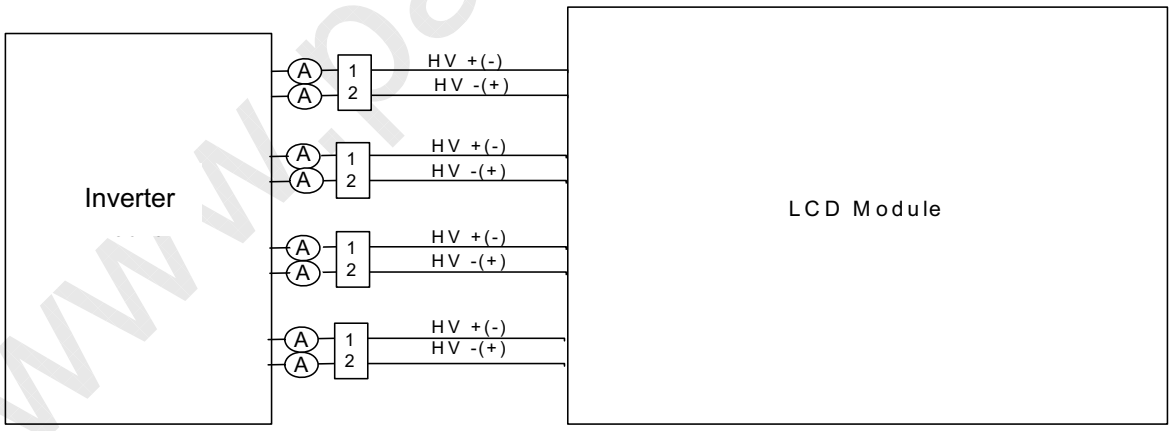
Note (3) The lamp frequency may produce interference with horizontal synchronous frequency of the display input signals, and it may result in line flow on the display. In order to avoid interference, the lamp frequency should be detached from the horizontal synchronous frequency and its harmonics as far as possible.

Note (4) The life time of a lamp is defined as when the brightness is larger than 50% of its original value and the effective discharge length is longer than 80% of its original length (Effective discharge length is defined as an area that has equal to or more than 70% brightness compared to the brightness at the center point of lamp.) as the time in which it continues to operate under the condition at Ta = 25 ±2 ℃ and I_L = 11.8~12.8 mArms.

Note (5) The power supply capacity should be higher than the total inverter power consumption P_{BL}. Since the pulse width modulation (PWM) mode was applied for backlight dimming, the driving current changed as PWM duty on and off. The transient response of power supply should be considered for the changing loading when inverter dimming.

Note (6) The measurement condition of Max. value is based on 31.5" backlight unit under input voltage 24V, average lamp current 12.6 mA and lighting 30 minutes later.

Note (7) 10% minimum duty ratio is only valid for electrical operation



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3.2.3 INVERTER INTERFACE CHARACTERISTICS

ITEM		SYMBOL	TEST CONDITION	MIN	TYPE	MAX	UNIT	NOTE
DET_5V		DET_5V	–	4.5	5.0	5.5	V	Abnormal
			–	0	–	0.8	V	Normal
On/Off Control Voltage	ON	V_{BLON}	–	3.3	–	5.3	V	
	OFF		–	0	–	0.8	V	
External PWM Control Voltage	HI	V_{EPWM}	–	3.5	–	5.3	V	Duty on
	LO		–	0	–	0.8	V	Duty off
Control Signal Rising Time		Tr	–	–	–	100	ms	
Control Signal Falling Time		Tf	–	–	–	100	ms	
VBL Rising Time		Tr1	–	30	–	–	ms	10%-90%V_{BL}
VBL Falling Time		Tf1	–	30	–	–	ms	
PWM Signal Rising Time		T_{PWMR}	–	–	–	100	us	
PWM Signal Falling Time		T_{PWMF}	–	–	–	100	us	
Input impedance		R_{IN}	–	1	–	–	MΩ	
PWM Delay Time		T_{PWM}	–	100		–	mS	
BLON Delay Time		T_{on}	–	300	–	–	mS	
		T_{on1}		300	–	–	mS	
BLON Off Time		T_{OFF}	–	300	–	–	mS	

Note (1) The Dimming signal should be valid before backlight turns on by BLON signal. It is inhibited to change the internal/external PWM signal during backlight turn on period.

Note (2) The power sequence and control signal timing are shown in the following figure. For a certain reason, the inverter has a possibility to be damaged with wrong power sequence and control signal timing.

Note (3) While system is turned ON or OFF, the power sequences must follow as below descriptions:

Turn ON sequence: VBL → PWM signal → BLON

Turn OFF sequence: BLOFF → PWM signal → VBL

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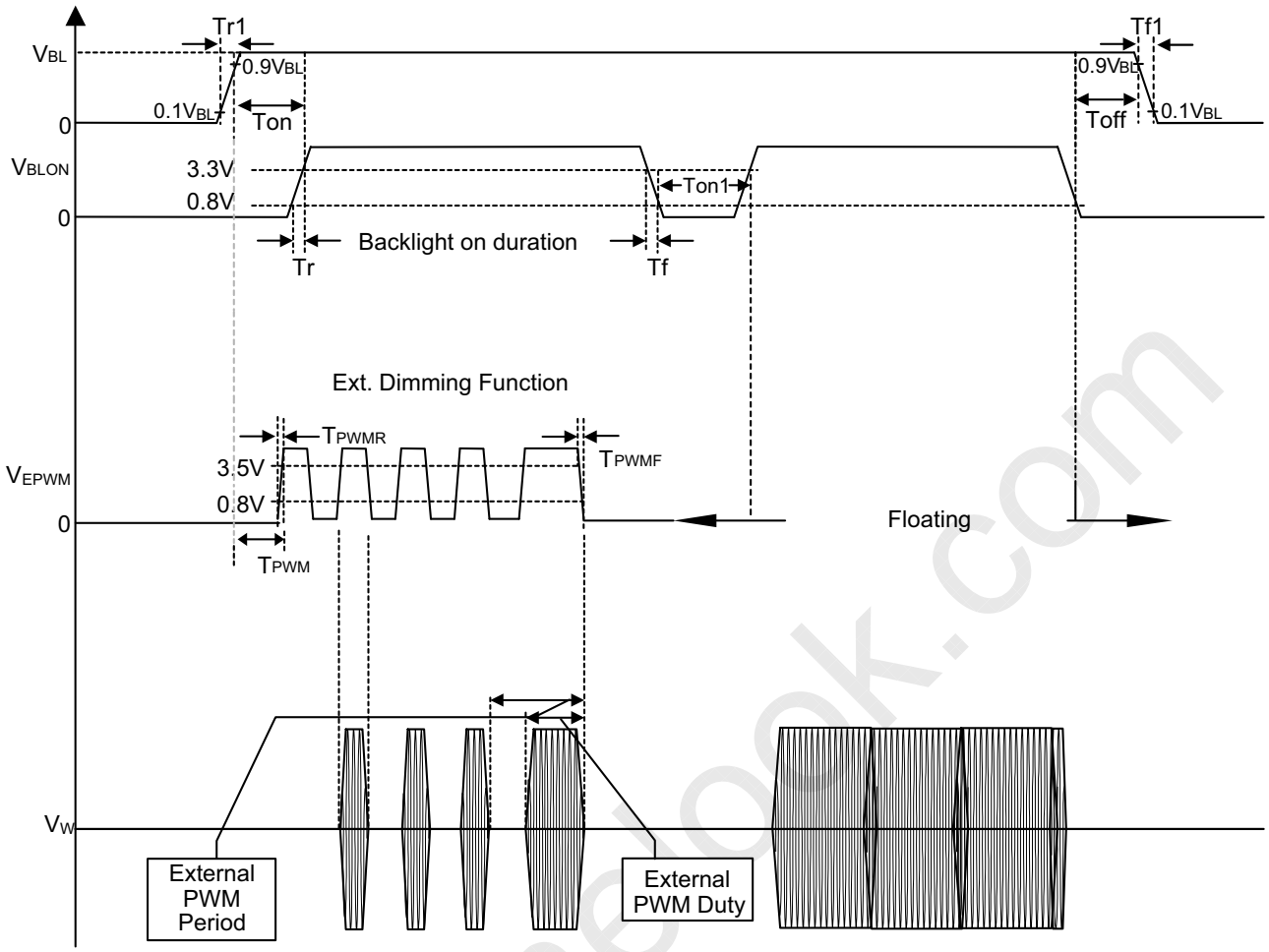

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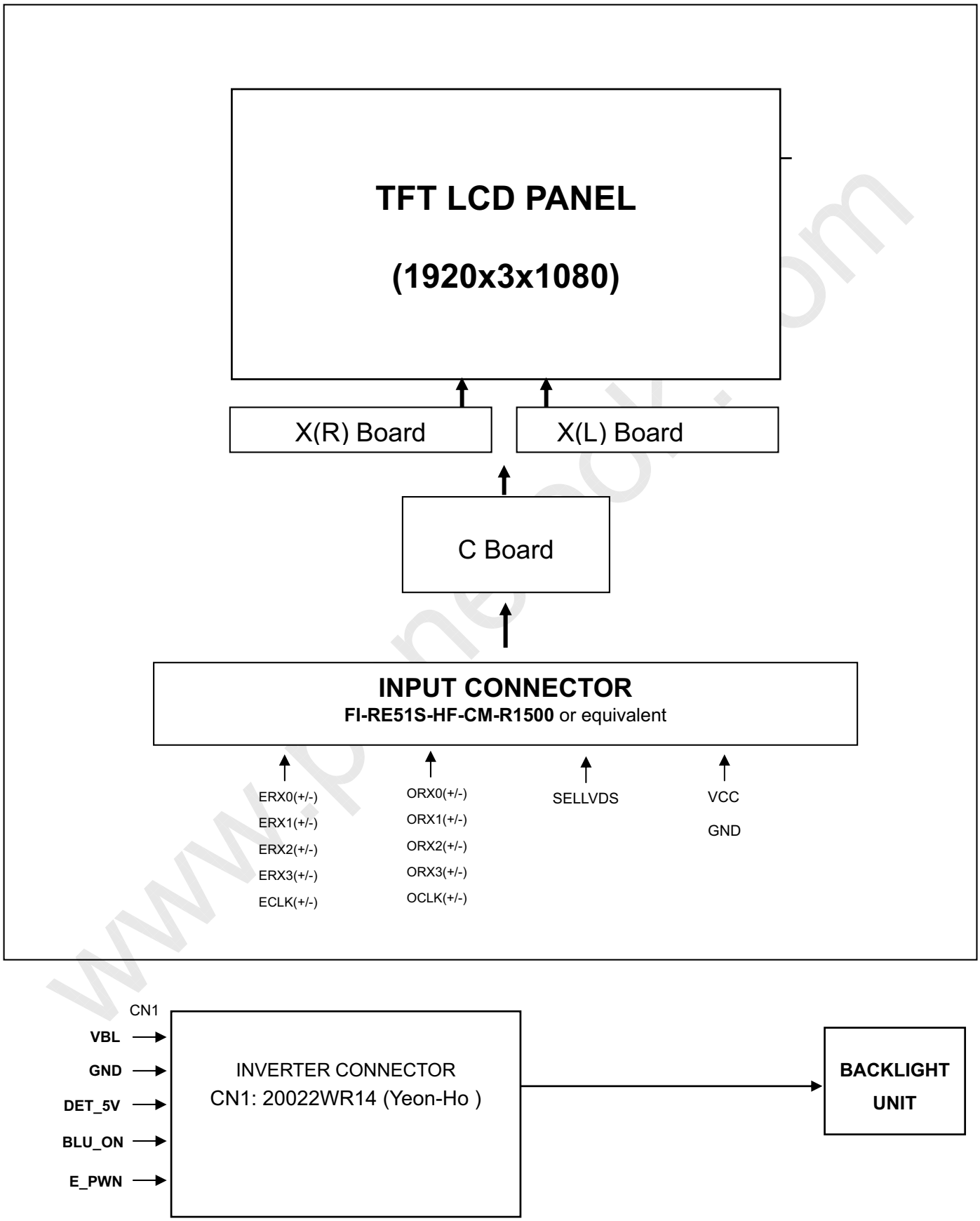
4. BLOCK DIAGRAM OF INTERFACE

4.1 TFT LCD MODULE



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5. INPUT TERMINAL PIN ASSIGNMENT

5.1 TFT LCD Module Input

CNF1 Connector Part No.: JAE Taiwan (台灣航空電子) FI-RE51S-HF-CM-R1500 or equivalent.

Pin	Name	Description	Note
1	VCC	+12V power supply	
2	VCC	+12V power supply	
3	VCC	+12V power supply	
4	VCC	+12V power supply	
5	VCC	+12V power supply	
6	N.C.	No Connection	(3)
7	GND	Ground	
8	GND	Ground	
9	GND	Ground	
10	ORX0-	Odd pixel Negative LVDS differential data input. Channel 0	(1)
11	ORX0+	Odd pixel Positive LVDS differential data input. Channel 0	
12	ORX1-	Odd pixel Negative LVDS differential data input. Channel 1	
13	ORX1+	Odd pixel Positive LVDS differential data input. Channel 1	
14	ORX2-	Odd pixel Negative LVDS differential data input. Channel 2	
15	ORX2+	Odd pixel Positive LVDS differential data input. Channel 2	
16	GND	Ground	
17	OCLK-	Odd pixel Negative LVDS differential clock input	(1)
18	OCLK+	Odd pixel Positive LVDS differential clock input.	
19	GND	Ground	
20	ORX3-	Odd pixel Negative LVDS differential data input. Channel 3	(1)
21	ORX3+	Odd pixel Positive LVDS differential data input. Channel 3	
22	N.C.	No Connection	(3)
23	N.C.	No Connection	
24	GND	Ground	
25	ERX0-	Even pixel Negative LVDS differential data input. Channel 0	(1)
26	ERX0+	Even pixel Positive LVDS differential data input. Channel 0	
27	ERX1-	Even pixel Negative LVDS differential data input. Channel 1	
28	ERX1+	Even pixel Positive LVDS differential data input. Channel 1	
29	ERX2-	Even pixel Negative LVDS differential data input. Channel 2	
30	ERX2+	Even pixel Positive LVDS differential data input. Channel 2	
31	GND	Ground	
32	ECLK-	Even pixel Negative LVDS differential clock input.	(1)
33	ECLK+	Even pixel Positive LVDS differential clock input.	

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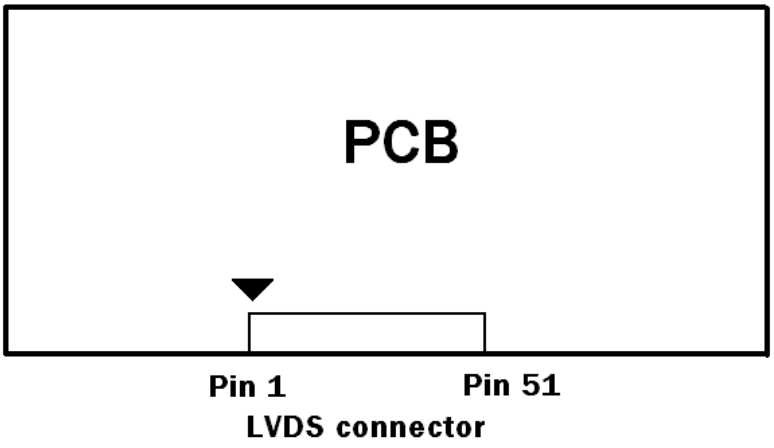
34	GND	Ground	
35	ERX3-	Even pixel Negative LVDS differential data input. Channel 3	(1)
36	ERX3+	Even pixel Positive LVDS differential data input. Channel 3	
37	N.C.	No Connection	(3)
38	N.C.	No Connection	
39	GND	Ground	
40	SCL	EEPROM Serial Clock	
41	N.C.	No Connection	(3)
42	N.C.	No Connection	(3)
43	WP	EEPROM Write Protection	
44	SDA	EEPROM Serial Data	
45	SELLVDS	LVDS data format selection	(4)(5)
46	N.C.	No Connection	(3)
47	N.C.	No Connection	
48	N.C.	No Connection	
49	N.C.	No Connection	
50	N.C.	No Connection	
51	N.C.	No Connection	

Note (1) Two pixel data send into the module for every clock cycle. The first pixel of the frame is odd pixel and the second pixel is even pixel

Note (2) LVDS connector pin order defined as follows



Note (3) Reserved for internal use. Please leave it open.

Note (4)

SELLVDS	Mode
L(default)	JEIDA
H	VESA

L: Connect to GND, H: Connect to +3.3V

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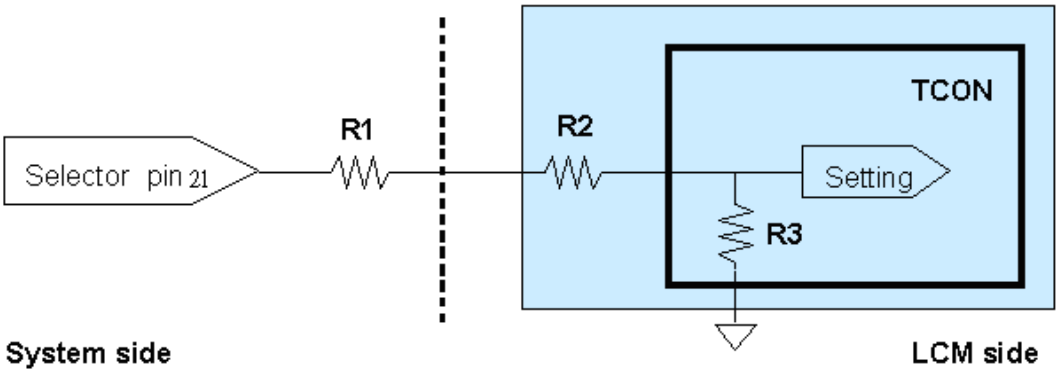
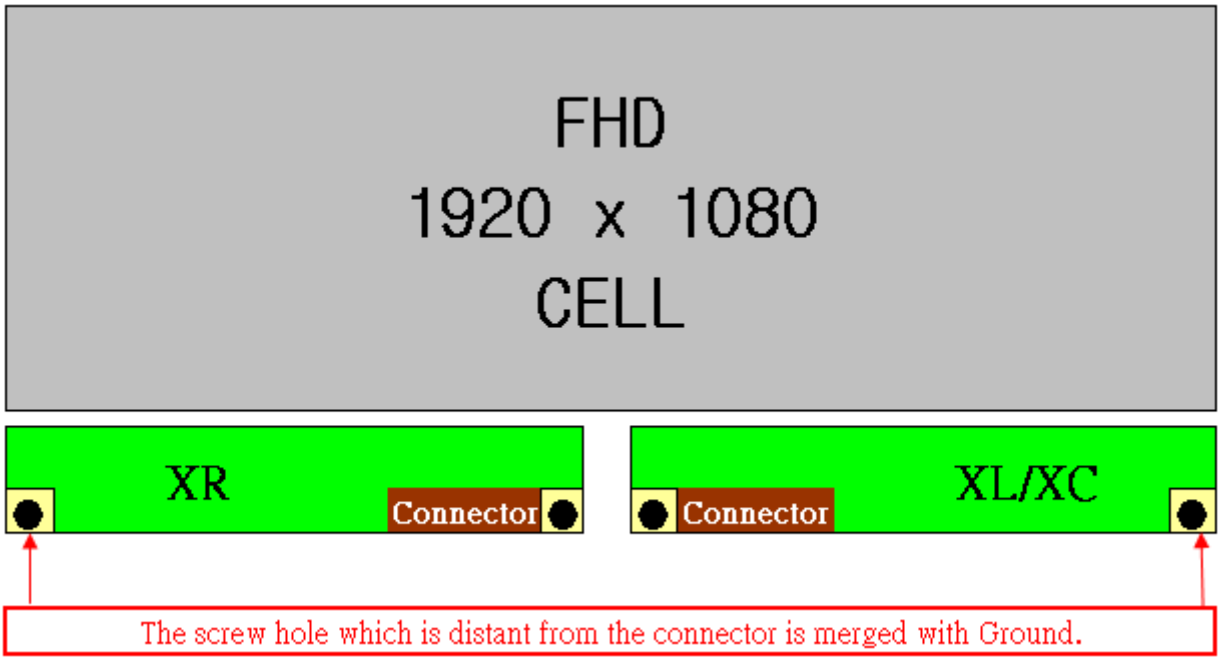
Note (5) LVDS signal pin connected to the LCM side has the following diagram.

R1 in the system side should be less than 1K Ohm. (R1 < 1K Ohm)



Note (6) The screw hole which is distant from the connector is merged with Ground



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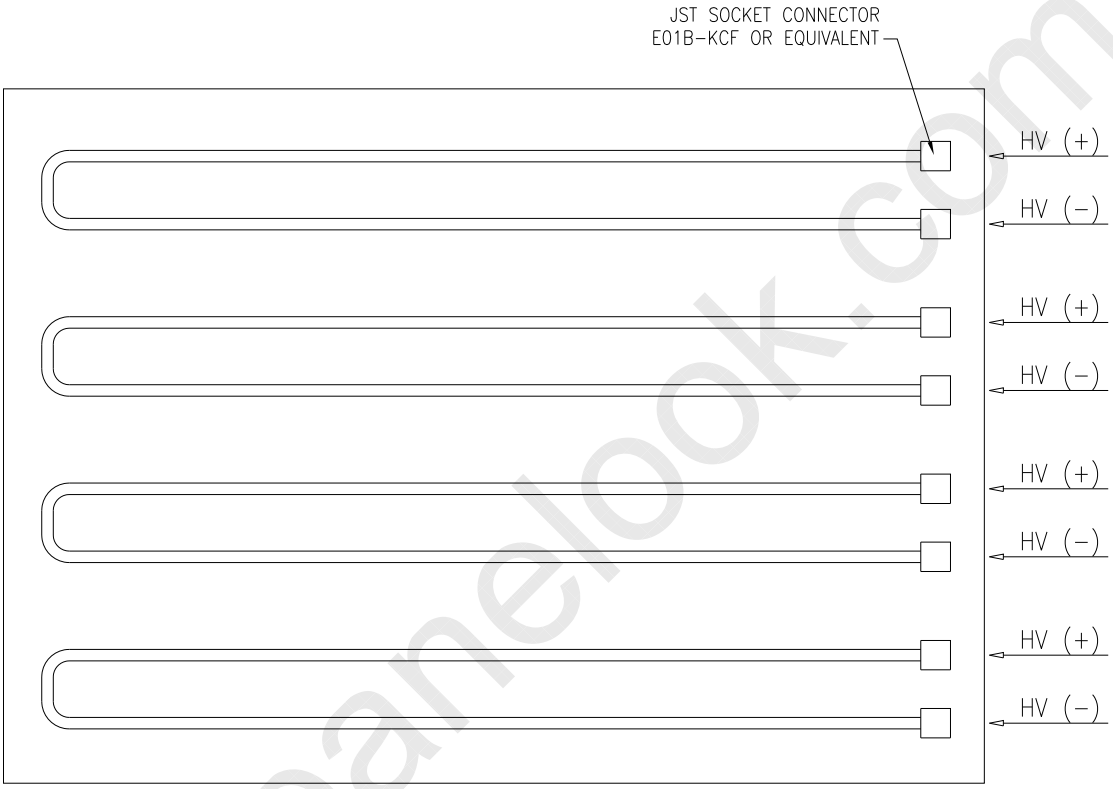
5.2 BACKLIGHT UNIT

The pin configuration for the housing and leader wire is shown in the table below.

CN2-CN5 (Socket Connector): E01B-KCF or equivalent

Pin No.	Symbol	Description	Remark
1	HV	High Voltage	
	HV	High Voltage	

Note (1) The backlight interface housing for high voltage side is a model E01B-KCF, manufactured by JST or equivalent.



5.3 INVERTER UNIT

CN1(Header): 20022WR14 (Yeon-Ho)

Pin No.	Symbol	Description
1	VBL	+24V Power input
2		
3		
4		
5		
6	GND	Ground
7		
8		
9		
10		
11	DET_5V	Check Lamp Ignition.
12	BLU_ON	BL ON/OFF
13	N.C.	No connect.
14	E_PWM	External PWM Control

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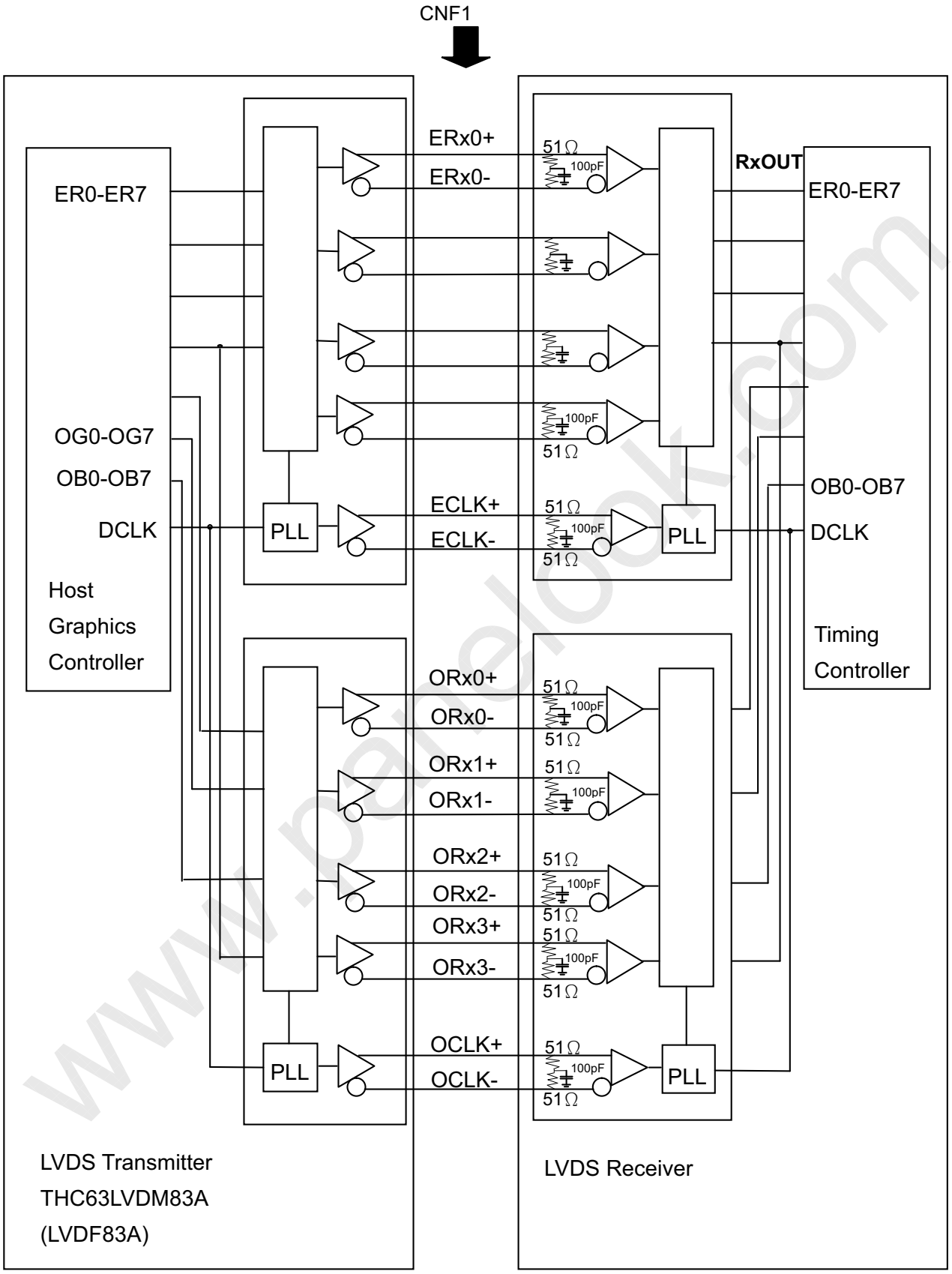
5.4 BLOCK DIAGRAM OF INTERFACE



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ER0~ER7 : Even pixel R data
EG0~EG7 : Even pixel G data
EB0~EB7 : Even pixel B data
OR0~OR7: Odd pixel R data
OG0~OG7: Odd pixel G data
OB0~OB7 : Odd pixel B data
DE : Data enable signal
DCLK : Data clock signal

Note (1) The system must have the transmitter to drive the module.

Note (2) LVDS cable impedance shall be 50 ohms per signal line or about 100 ohms per twist-pair line when it is used differentially.

Note (3) Two pixel data send into the module for every clock cycle. The first pixel of the frame is odd pixel and the second pixel is even pixel.

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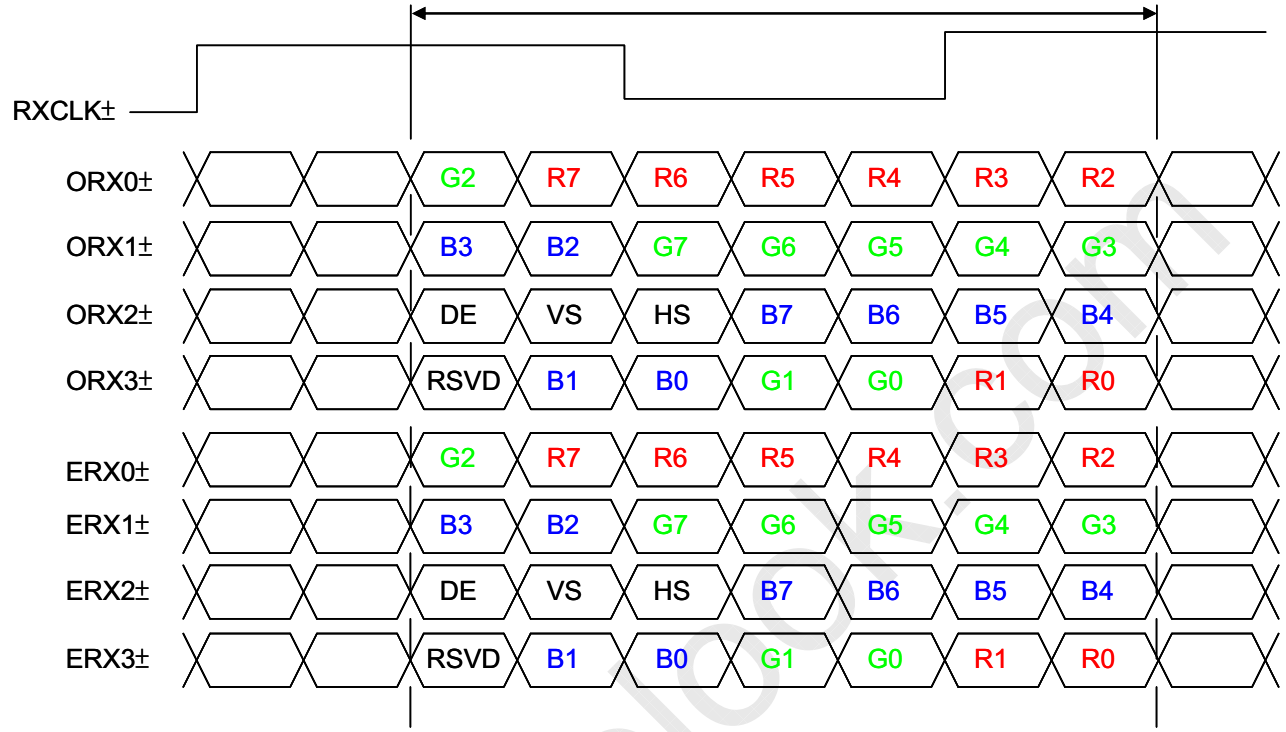
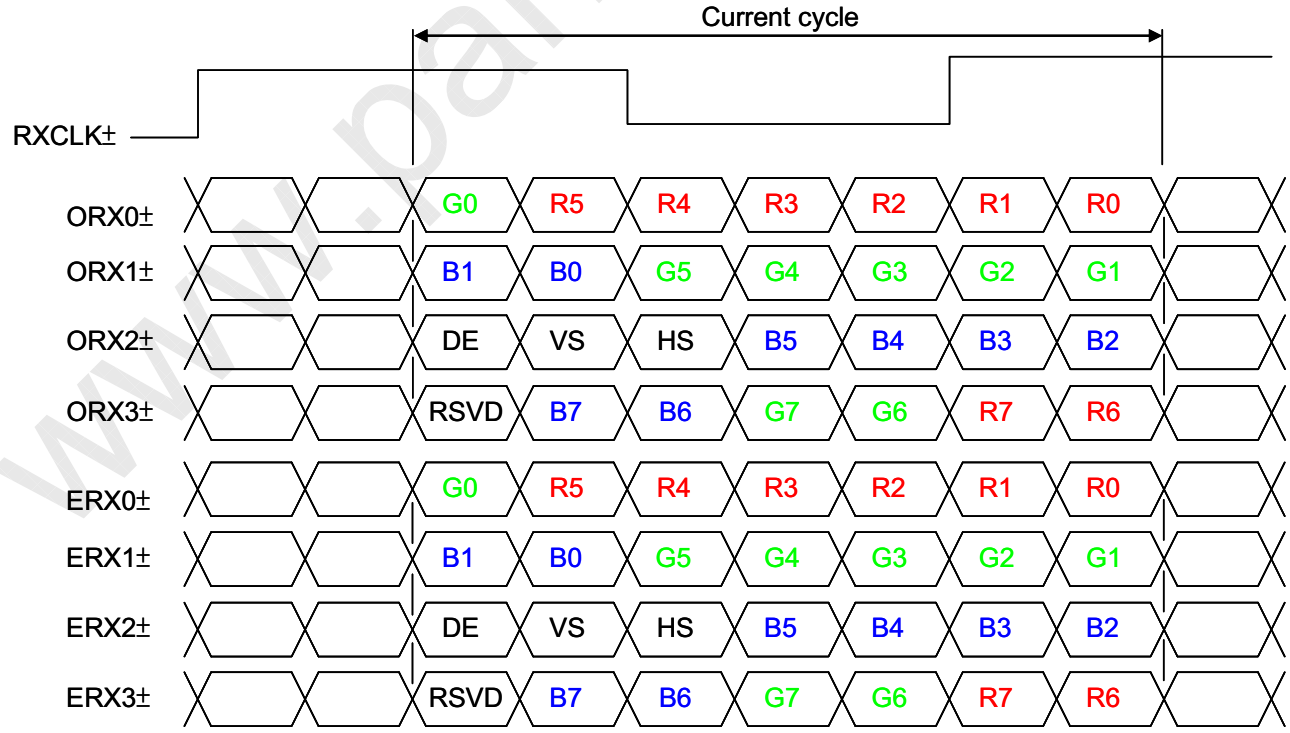
5.5 LVDS INTERFACE

JEDIA Format：SELLVDS=L or Open



VESA Format：SELLVDS=H



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R0~R7: Pixel R Data (7; MSB, 0; LSB)

G0~G7: Pixel G Data (7; MSB, 0; LSB)

B0~B7: Pixel B Data (7; MSB, 0; LSB)

DE: Data enable signal

DCLK: Data clock signal

Notes (1) RSVD (reserved) pins on the transmitter shall be “H” or “L”.

5.6 COLOR DATA INPUT ASSIGNMENT

The brightness of each primary color (red, green and blue) is based on the 8-bit gray scale data input for the color. The higher the binary input, the brighter the color. The table below provides the assignment of the color versus data input.

Color		Data Signal																							
		Red								Green								Blue							
		R7	R6	R5	R4	R3	R2	R1	R0	G7	G6	G5	G4	G3	G2	G1	G0	B7	B6	B5	B4	B3	B2	B1	B0
Basic Colors	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Green	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
	Blue	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
	Cyan	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
	Magenta	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
	Yellow	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
	White	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Gray Scale Of Red	Red (0) / Dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red (1)	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red (2)	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	Red (253)	1	1	1	1	1	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red (254)	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red (255)	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Gray Scale Of Green	Green (0) / Dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Green (1)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0
	Green (2)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	Green (253)	0	0	0	0	0	0	0	0	1	1	1	1	1	1	0	1	0	0	0	0	0	0	0	0
	Green (254)	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0
	Green (255)	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0

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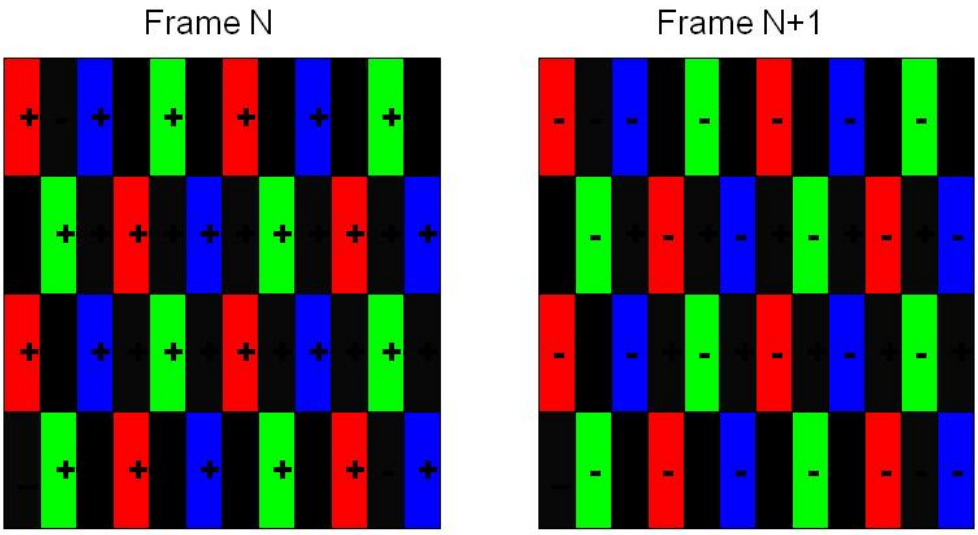
Gray Scale Of Blue	Blue (0) / Dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Blue (1)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
	Blue (2)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	Blue (253)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	0	1
	Blue (254)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	0
	Blue (255)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1

Note (1) 0: Low Level Voltage, 1: High Level Voltage

5.7 FLICKER (Vcom) ADJUSTMENT

(1) Adjustment Pattern:

Inversion pattern was shown as below. If customer need below pattern, please directly contact with Account FAE.



(2) Adjustment method: (Digital V-com)

Programmable memory IC is used for Digital V-com adjustment in this model. CMI provide Auto Vcom tools to adjust Digital V-com.The detail connection and setting instruction, please directly contact with Account FAE or refer CMI Auto V-com adjustment OI.

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6. INTERFACE TIMING

6.1 INPUT SIGNAL TIMING SPECIFICATIONS

(Ta = 25 ± 2 ºC)

The input signal timing specifications are shown as the following table and timing diagram.

Signal	Item	Symbol	Min.	Typ.	Max.	Unit	Note
LVDS Receiver Clock	Frequency	F_{clkin} (=1/TC)	60	74.25	80	MHz	
	Input cycle to cycle jitter	T_{rcl}	—	—	200	ps	(3)
	Spread spectrum modulation range	F_{clkin_mod}	F_{clkin}-2%	—	F_{clkin}+2%	MHz	(4)
	Spread spectrum modulation frequency	F_{SSM}	—	—	200	KHz	
LVDS Receiver Data	Setup Time	Tlvsu	600	—	—	ps	(5)
	Hold Time	Tlvhd	600	—	—	ps	
Vertical Active Display Term	Frame Rate	F_{r5}	47	50	53	Hz	
		F_{r6}	57	60	63	Hz	
	Total	Tv	1090	1125	1480	Th	Tv=Tvd+Tvb
	Display	Tvd	1080	1080	1080	Th	
	Blank	Tvb	10	45	400	Th	
Horizontal Active Display Term	Total	Th	1030	1100	1325	Tc	Th=Thd+Thb
	Display	Thd	960	960	960	Tc	
	Blank	Thb	70	140	365	Tc	

Note (1) Please make sure the range of pixel clock has follow the below equation：

Fclkin(max) ≧ Fr6 × Tv × Th

Fr5 × Tv × Th ≧ Fclkin(min)

Note (2) This module is operated in DE only mode and please follow the input signal timing diagram below：

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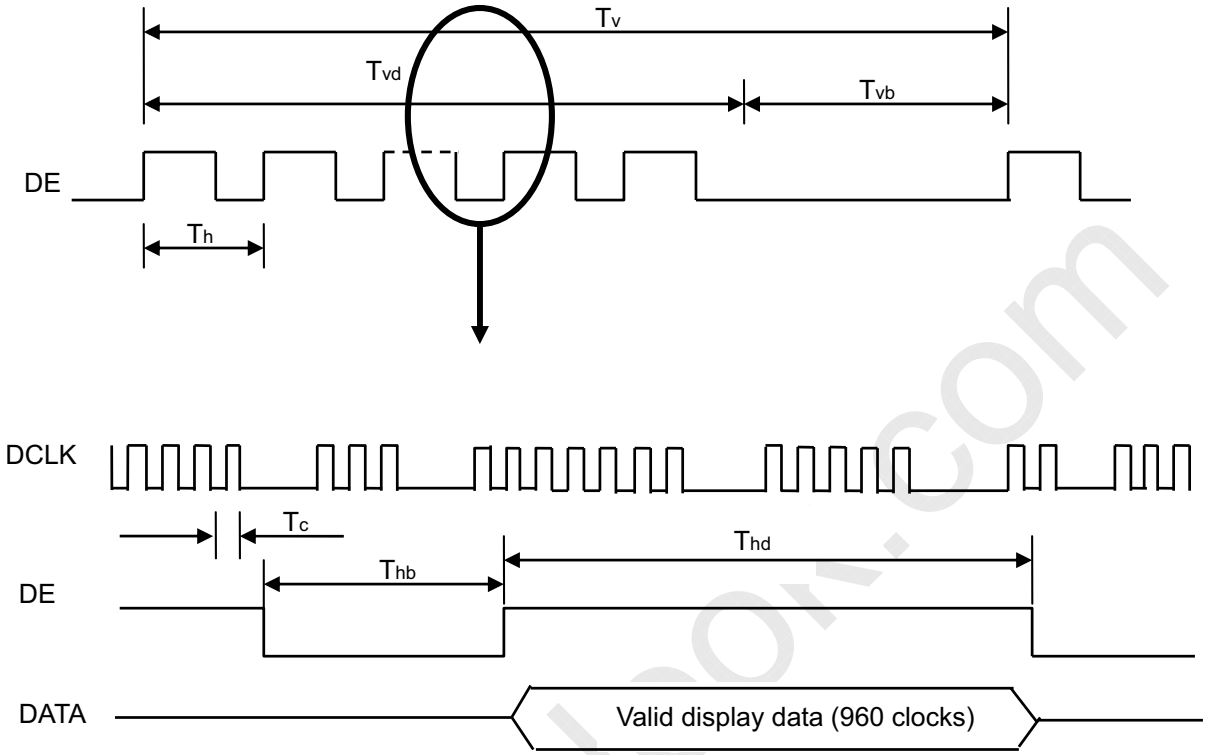
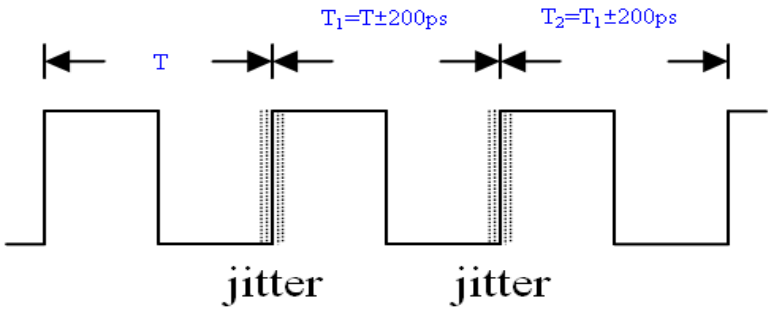
INPUT SIGNAL TIMING DIAGRAM



Note (3) The input clock cycle-to-cycle jitter is defined as below figures. Trcl = I T_1 – TI



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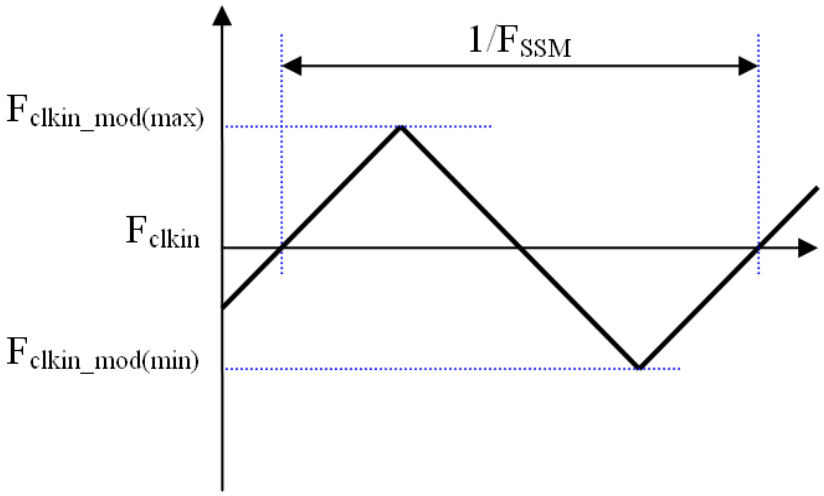
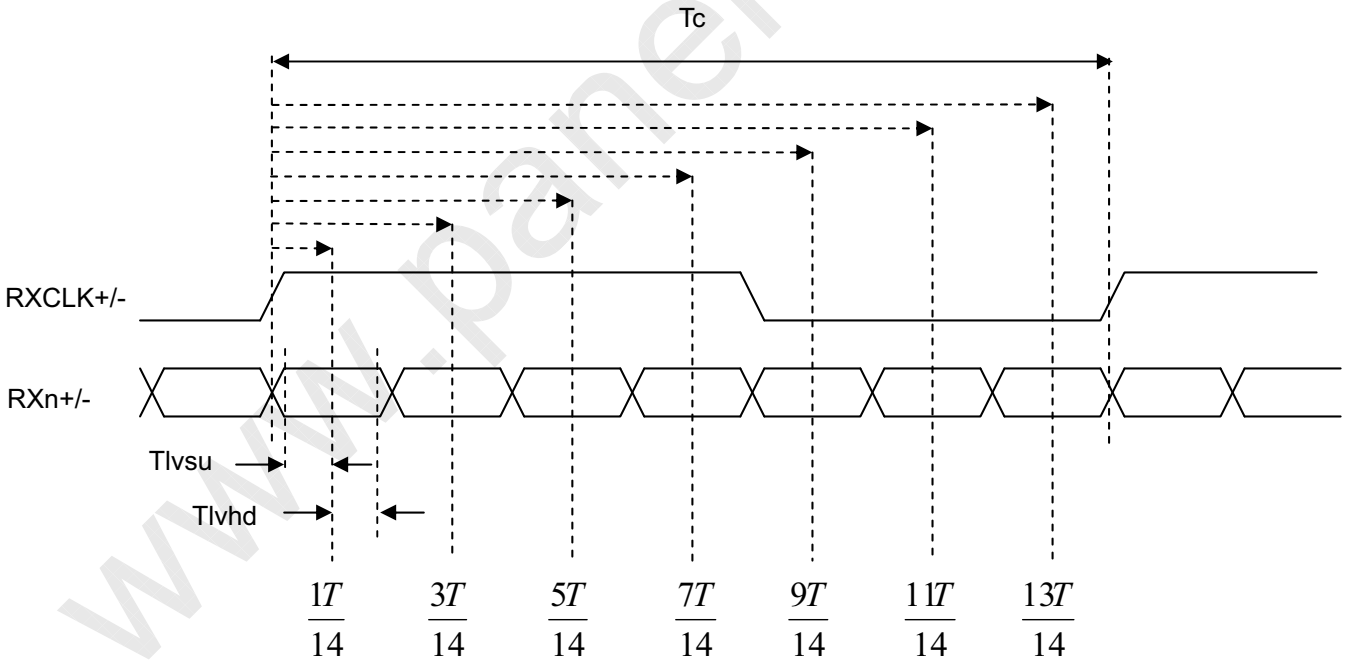
Note (4) The SSCG (Spread spectrum clock generator) is defined as below figures.



Note (5) The LVDS timing diagram and setup/hold time is defined and showing as the following figures.

LVDS RECEIVER INTERFACE TIMING DIAGRAM



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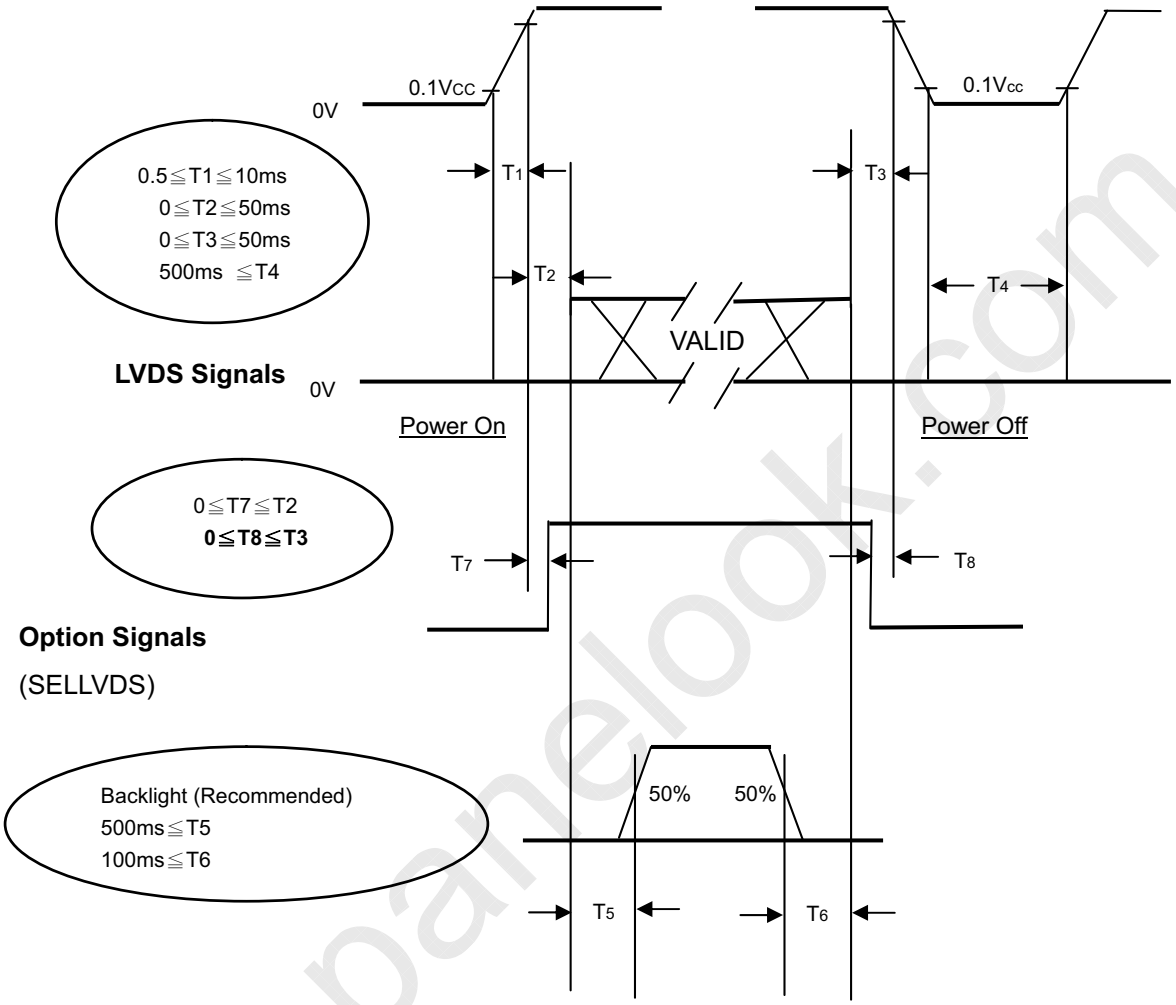
6.2 POWER ON/OFF SEQUENCE

(Ta = 25 ± 2 ºC)

To prevent a latch-up or DC operation of LCD module, the power on/off sequence should be as the diagram below.



Power ON/OFF Sequence

Note (1) The supply voltage of the external system for the module input should follow the definition of Vcc.

Note (2) Apply the lamp voltage within the LCD operation range. When the backlight turns on before the LCD operation or the LCD turns off before the backlight turns off, the display may momentarily become abnormal screen.

Note (3) In case of VCC is in off level, please keep the level of input signals on the low or high impedance.

Note (4) T4 should be measured after the module has been fully discharged between power off and on period.

Note (5) Interface signal shall not be kept at high impedance when the power is on.

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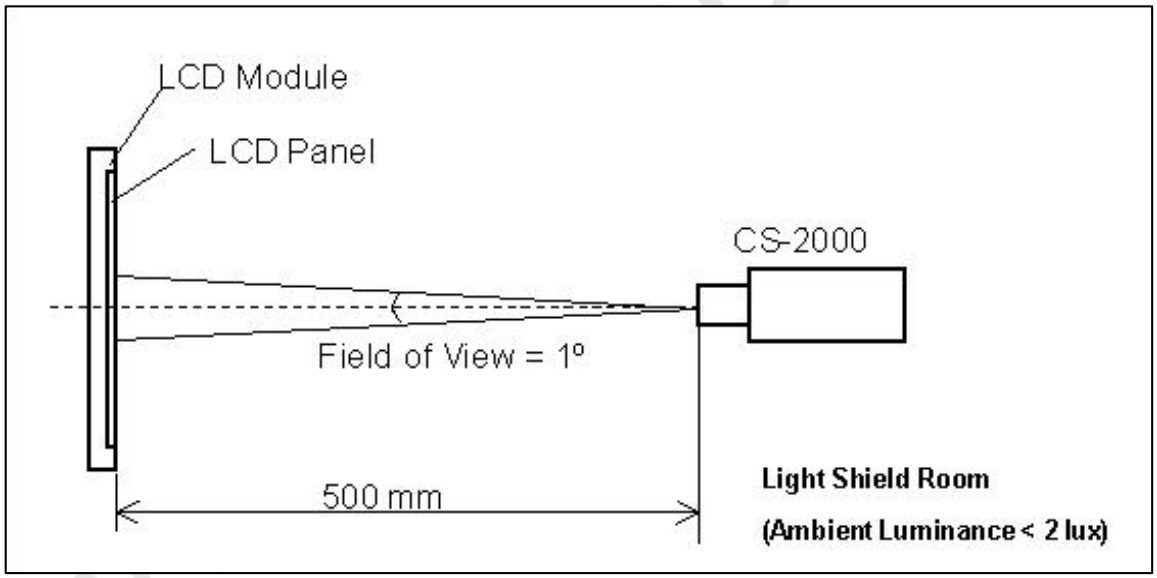
7. OPTICAL CHARACTERISTICS

7.1 TEST CONDITIONS

Item	Symbol	Value	Unit
Ambient Temperature	Ta	25±2	°C
Ambient Humidity	Ha	50±10	%RH
Supply Voltage	VCC	12	V
Input Signal	According to typical value in "3. ELECTRICAL CHARACTERISTICS"		
Lamp Current	IL	12.3±0.5	mA
Oscillating Frequency (Inverter)	FW	58±3	KHz
Vertical Frame Rate	Fr	60	Hz

The LCD module should be stabilized at given temperature for 1 hour to avoid abrupt temperature change during measuring in a windless room.



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7.2 OPTICAL SPECIFICATIONS

The relative measurement methods of optical characteristics are shown in 7.2. The following items should be measured under the test conditions described in 7.1 and stable environment shown in 7.1.

Item		Symbol	Condition	Min.	Typ.	Max.	Unit	Note
Contrast Ratio		CR	θx=0°, θy =0° Viewing angle at normal direction	4000	6000	-	-	(2)
Response Time (VA)		Gray to gray		-	8.5	-	ms	(3)
Center Luminance of White		L_C		360	450	-	cd/m^2	(4)
White Variation		δW		-	-	1.3	-	(6)
Cross Talk		CT		-	-	4	%	(5)
Color Chromaticity	Red	Rx		Typ. -0.03	0.642	Typ. +0.03	-	-
		Ry			0.326		-	
	Green	Gx			0.292		-	
		Gy			0.604		-	
	Blue	Bx			0.143		-	
		By			0.064		-	
	White	Wx			0.281		-	
		Wy			0.288		-	
	Color Gamut	C.G		-	72	-	%	NTSC
Viewing Angle	Horizontal	θx+	CR≥20 (VA)	80	88	-	Deg.	(1)
		θx-		80	88	-		
	Vertical	θY+		80	88	-		
		θY-		80	88	-		

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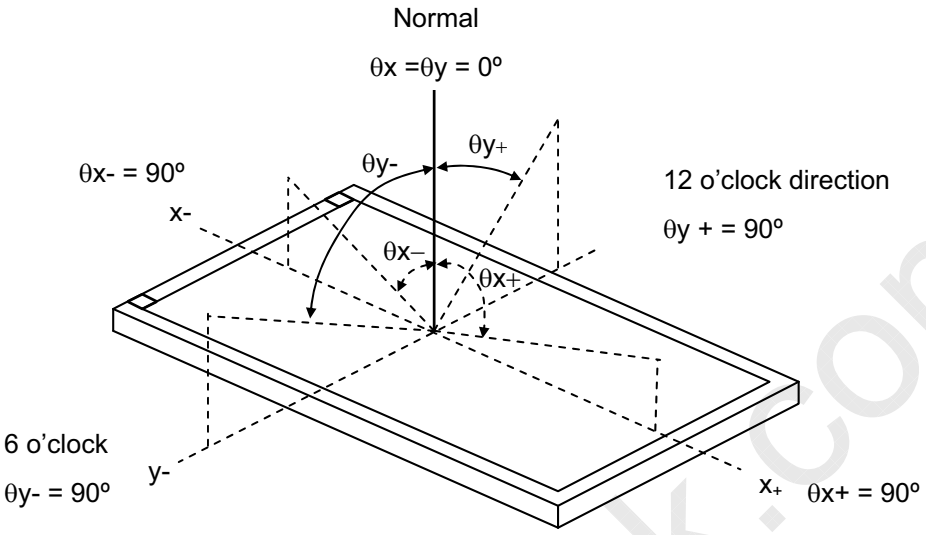
Note (1) Definition of Viewing Angle (θx, θy) :

Viewing angles are measured by Conoscope Cono-80 (or Eldim EZ-Contrast 160R)



Note (2) Definition of Contrast Ratio (CR) :

The contrast ratio can be calculated by the following expression.

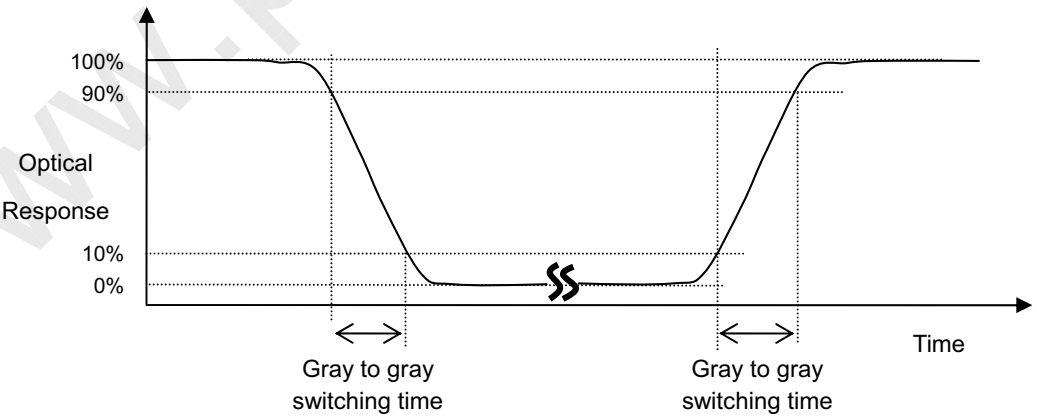
$$\text{Contrast Ratio (CR)} = \frac{\text{Surface Luminance of L255}}{\text{Surface Luminance of L0}}$$

L255: Luminance of gray level 255

L 0: Luminance of gray level 0

CR = CR (5), where CR (X) is corresponding to the Contrast Ratio of the point X at the figure in Note (6).

Note (3) Definition of Gray-to-Gray Switching Time:



The driving signal means the signal of gray level 0, 31, 63, 95, 127, 159, 191, 223 and 255.

Gray to gray average time means the average switching time of gray level 0, 31, 63, 95, 127, 159, 191, 223 and 255. to each other.

Note (4) Definition of Luminance of White (L_C):

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Measure the luminance of gray level 255 at center point and 5 points

L_C = L (5), where L (X) is corresponding to the luminance of the point X at the figure in Note (6).

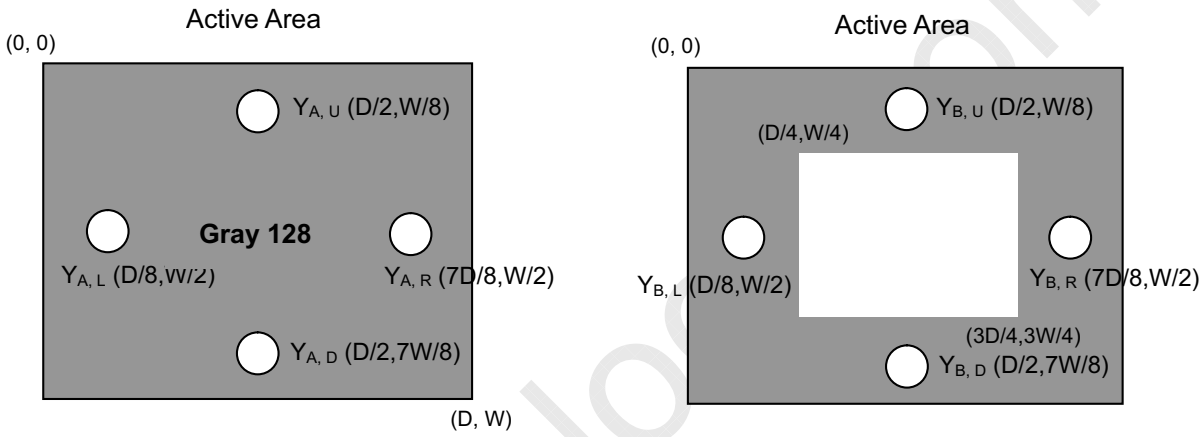
Note (5) Definition of Cross Talk (CT):

$CT = | Y_B - Y_A | / Y_A \times 100$ (%)

Where:

Y_A = Luminance of measured location without gray level 255 pattern (cd/m2)

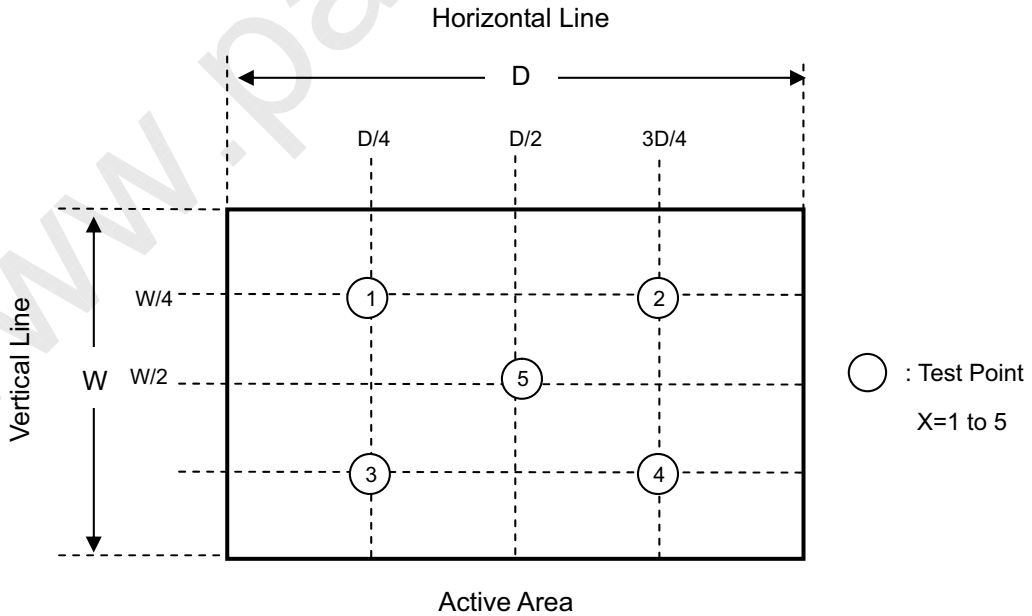
Y_B = Luminance of measured location with gray level 255 pattern (cd/m2)



Note (6) Definition of White Variation (δW):

Measure the luminance of gray level 255 at 5 points

δW = Maximum [L (1), L (2), L (3), L (4), L (5)] / Minimum [L (1), L (2), L (3), L (4), L (5)]



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PRECAUTIONS

8.1 ASSEMBLY AND HANDLING PRECAUTIONS

[1] Do not apply rough force such as bending or twisting to the module during assembly.

[2] It is recommended to assemble or to install a module into the user's system in clean working areas. The dust and oil may cause electrical short or worsen the polarizer.

[3] Do not apply pressure or impulse to the module to prevent the damage of LCD panel and Backlight.

[4] Always follow the correct power-on sequence when the LCD module is turned on. This can prevent the damage and latch-up of the CMIS LSI chips.

[5] Bezel of Set can not press or touch the panel surface. It will make light leakage or scrape.

[6] Do not plug in or pull out the I/F connector while the module is in operation.

[7] Do not disassemble the module.

[8] Use a soft dry cloth without chemicals for cleaning, because the surface of polarizer is very soft and easily scratched.

[9] Moisture can easily penetrate into LCD module and may cause the damage during operation.

[10] When storing modules as spares for a long time, the following precaution is necessary.

[10.1] Do not leave the module in high temperature, and high humidity for a long time. It is highly recommended to store the module with temperature from 0 to 35℃at normal humidity without condensation.

[10.2] The module shall be stored in dark place. Do not store the TFT-LCD module in direct sunlight or fluorescent light.

[11] When ambient temperature is lower than 10ºC, the display quality might be reduced. For example, the response time will become slow, and the starting voltage of CCFL will be higher than that of room temperature.

8.2 SAFETY PRECAUTIONS

[1] The startup voltage of a Backlight is approximately 1000 Volts. It may cause an electrical shock while assembling with the inverter. Do not disassemble the module or insert anything into the Backlight unit.

[2] If the liquid crystal material leaks from the panel, it should be kept away from the eyes or mouth. In case of contact with hands, skin or clothes, it has to be washed away thoroughly with soap.

[3] After the module's end of life, it is not harmful in case of normal operation and storage.

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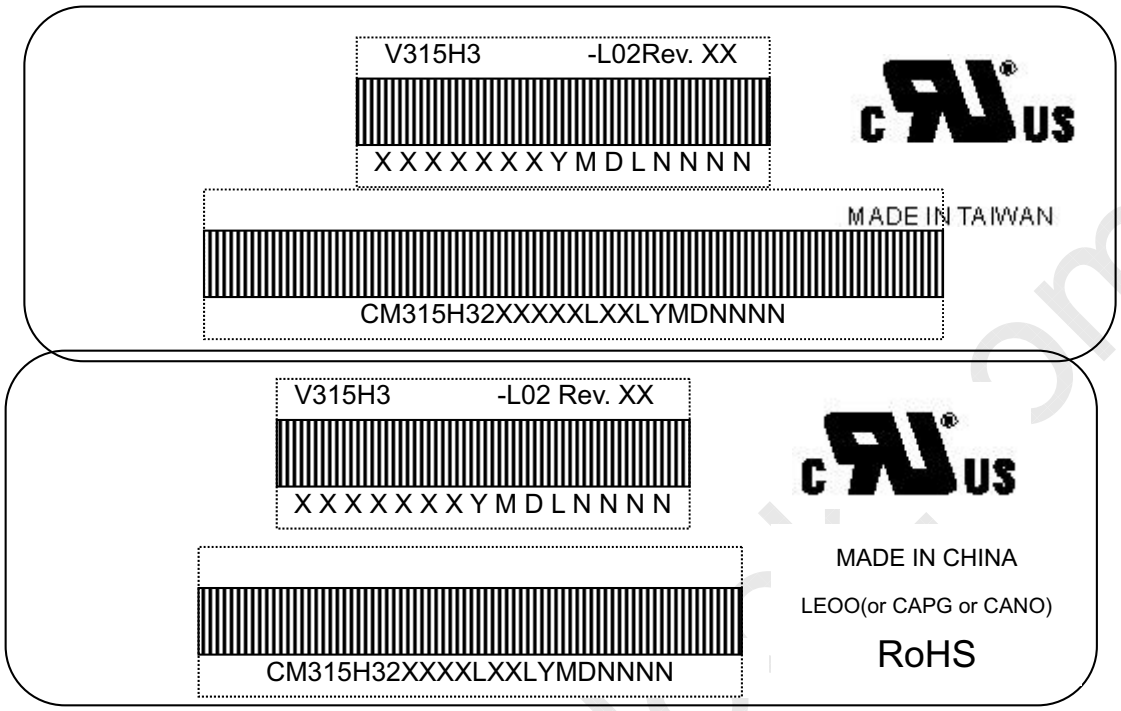
9. DEFINITION OF LABELS

9.1 CMI MODULE LABEL

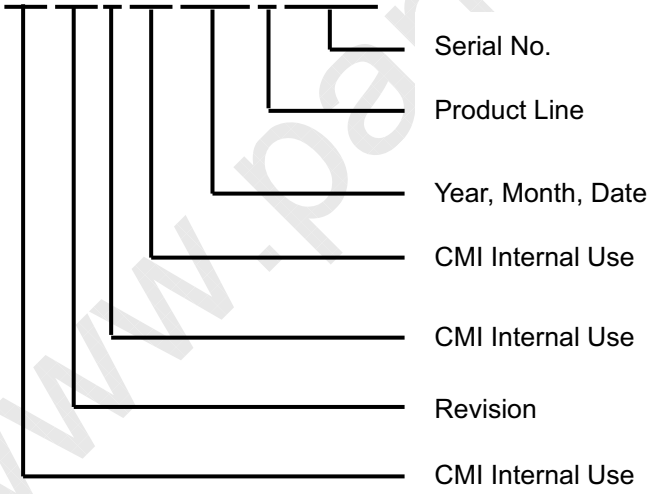
The barcode nameplate is pasted on each module as illustration, and its definitions are as following explanation.



Model Name: V315H3-L02

Revision: Rev. XX, for example: A0, A1… B1, B2… or C1, C2…etc.

Serial ID: X X X X X X Y M D L N N N N



Serial ID includes the information as below:

Manufactured Date:

Year : 2001=1, 2002=2, 2003=3, 2004=4…2010=0, 2011=1, 2012=2…

Month: 1~9, A~C, for Jan. ~ Dec.

Day: 1~9, A~Y, for 1st to 31st, exclude I ,O, and U.

Revision Code : Cover all the change

Serial No. : Manufacturing sequence of product

Product Line : 1 → Line1, 2 → Line 2, …etc.

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10. PACKAGING

10.1 PACKAGING SPECIFICATIONS

(1) 5 LCD TV modules / 1 Box

(2) Box dimensions : 826(L) X 376 (W) X 540 (H)

(3) Weight : approximately 30Kg (5 modules per box)

a.Panel module each pcs : 5.211 kg

b.Panel Packing Box

-Cushion : 0.494 kg (5 pcs per box)

-Carton : 2.3 kg

-Panel : 5.211 kg x 5pcs =26.055 kg

-Panel Packing Box Total (1 Box) =28.849 kg

c.Total Packing weight

1)For Vessel shipment Pallet (1 Pallet =6 Box or 9 Box)

-Pallet weight : 12 kg

-Pallet Cushion : 2.96 kg or 4.44 kg

-Pallet Packing Total = 185.09 kg or 271.6 kg

2)For Air shipment Pallet (1 Pallet =6 Box)

-Pallet weight : 12 kg

-Pallet Cushion : 2.96 kg

-Pallet Packing Total =185.09 kg

10.2 PACKAGING METHOD

Figures 10-1 and 10-2 are the packing method

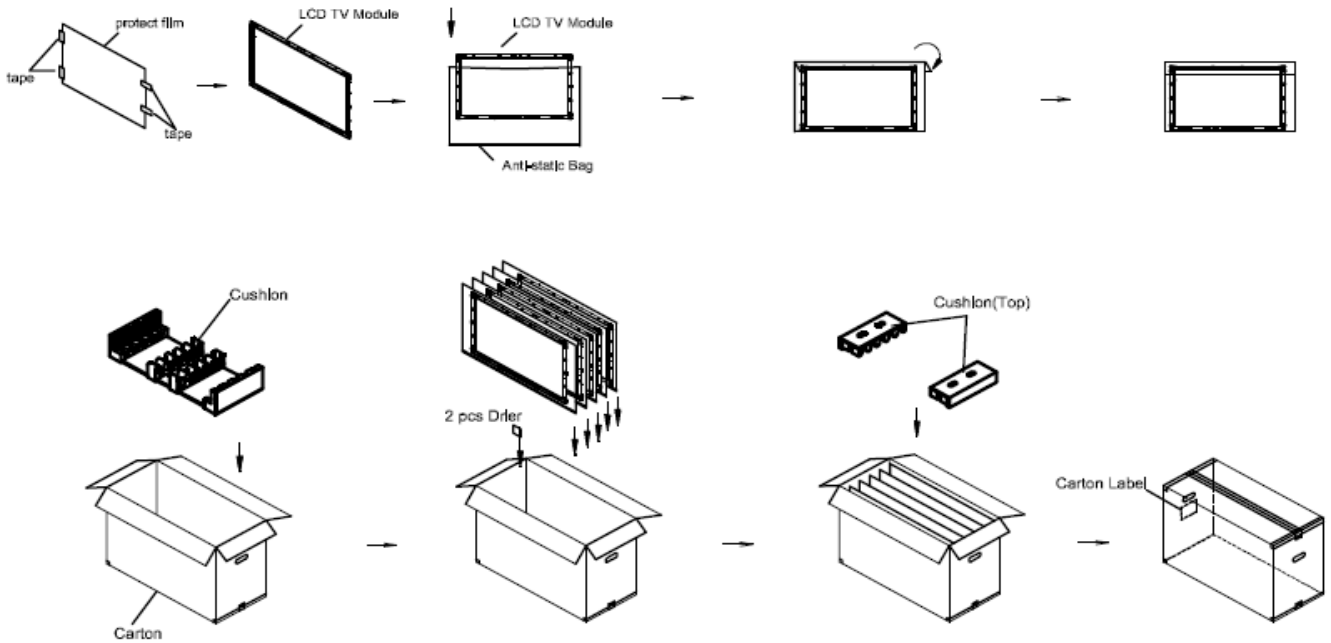

Figure 10-1 packing method

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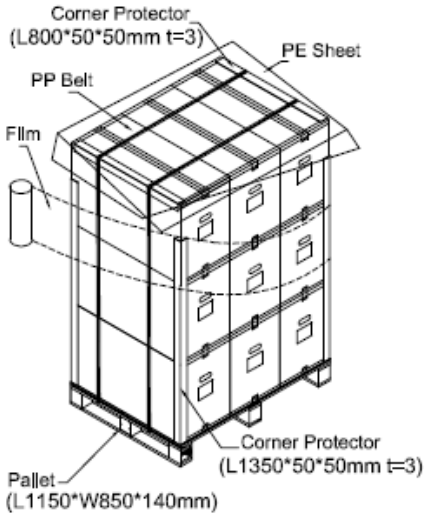
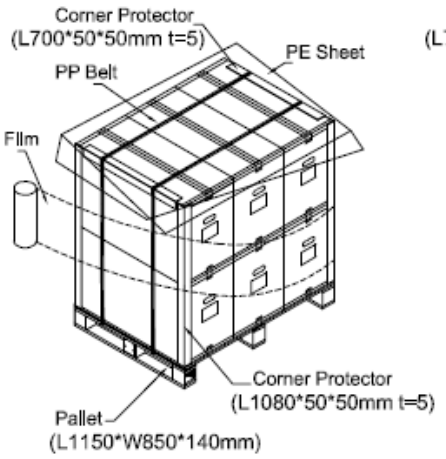
Sea / Land Transportation (40ft Container)



Air Transportation



Sea / Land Transportation (40ft HQ Container)

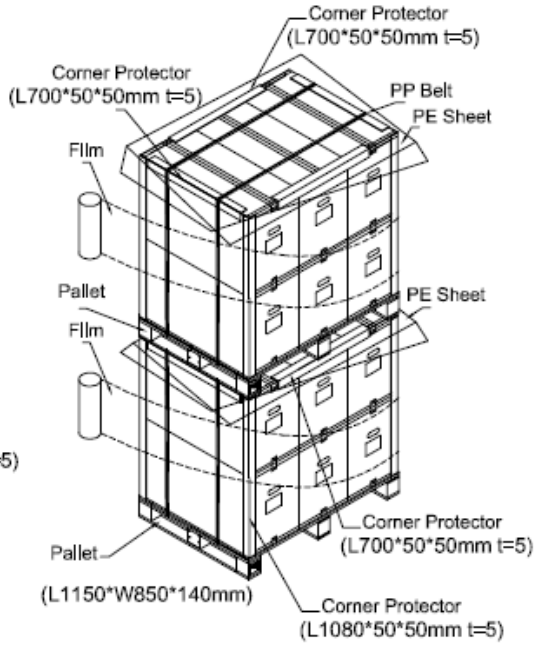


Figure 10-2 packing method

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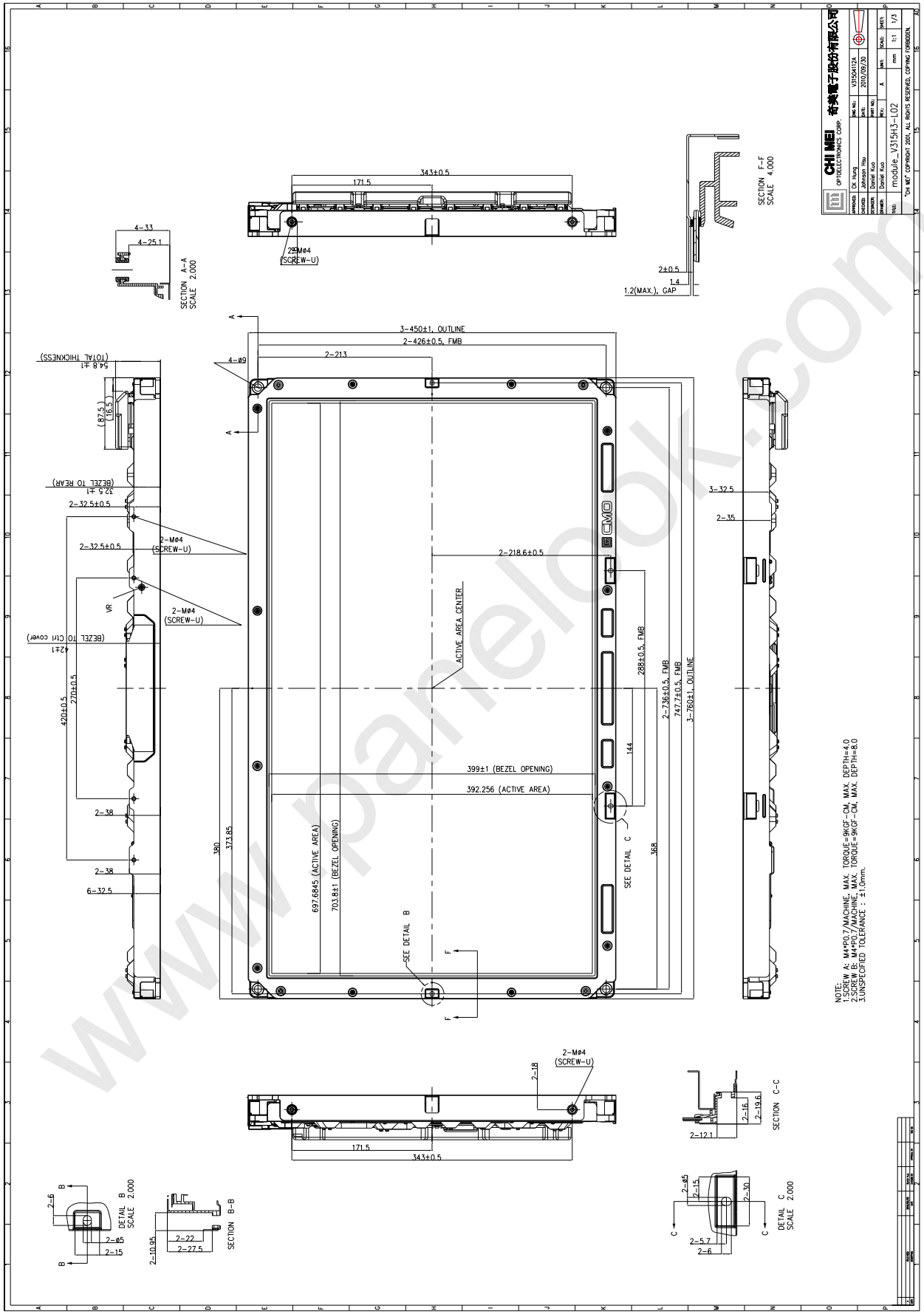
11. MECHANICAL CHARACTERISTIC



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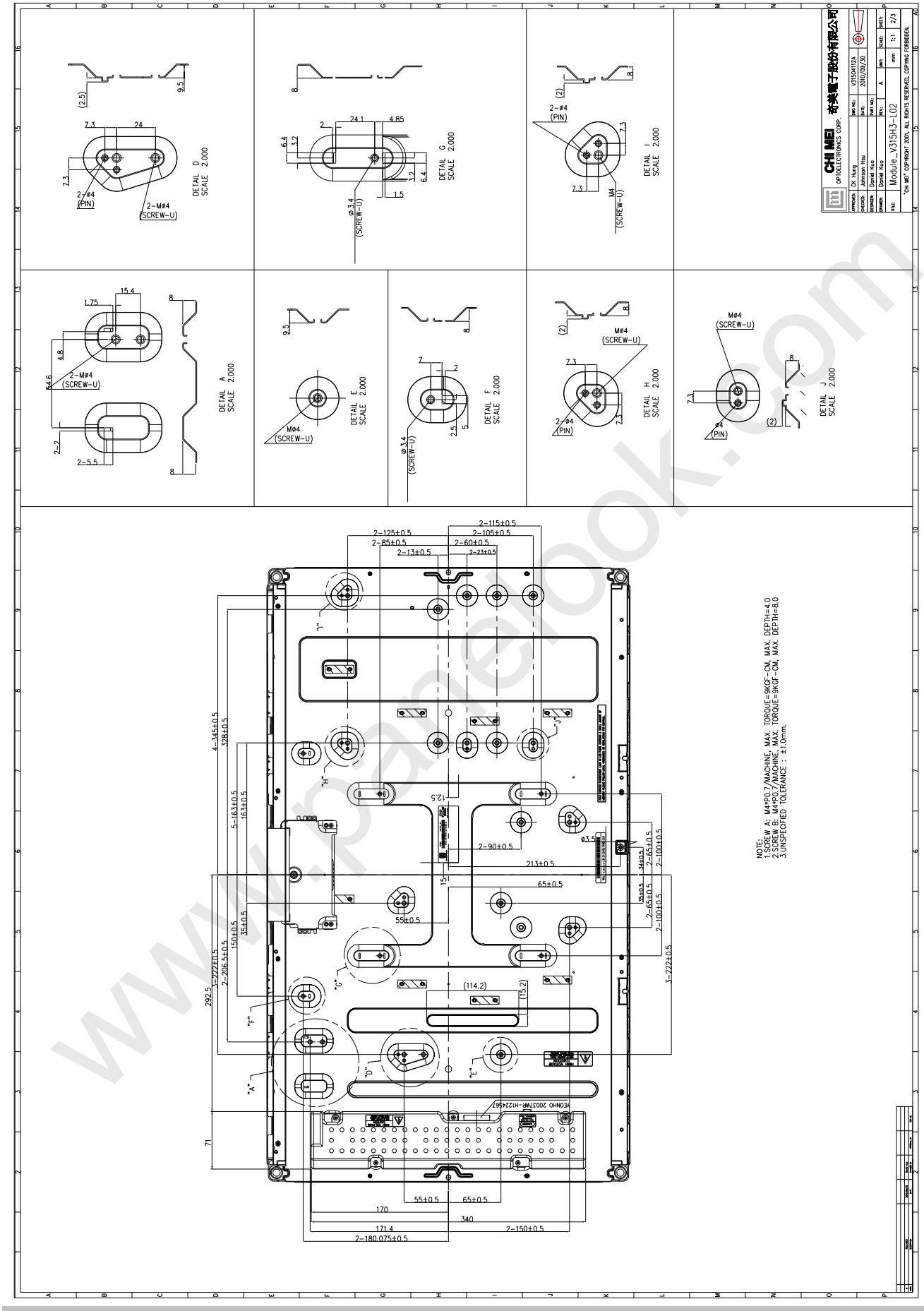

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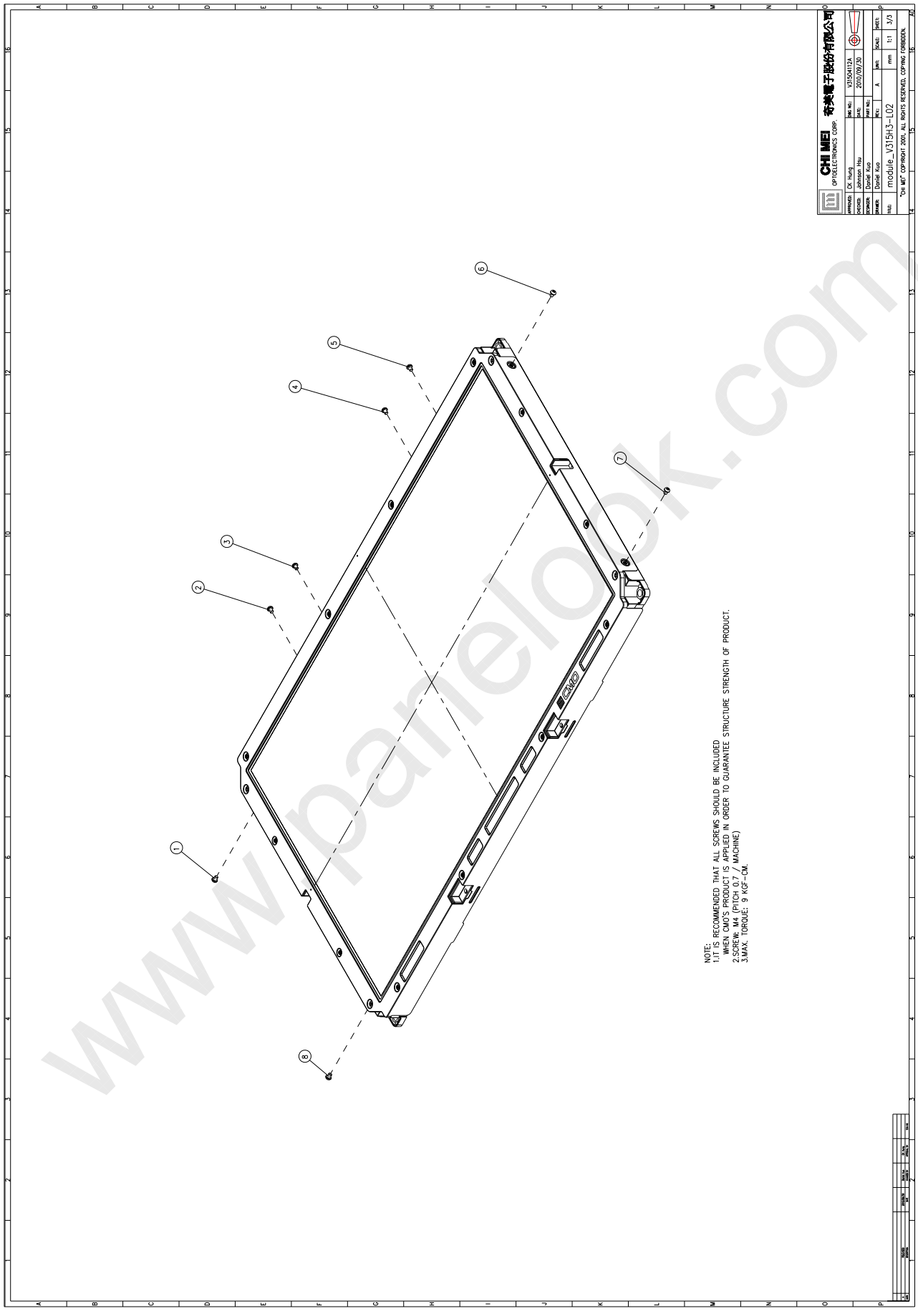

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